a contact hole formed within said pad trench to electrically connect said conductive film to said further conductive film, wherein said contact hole and said further conductive film substantially suppress an increase in electrical resistance in said pad trench due to formation of said protrusion.

9. (Amended) A semiconductor device according to claim 8, wherein said protrusion is formed not to divide said conductive film buried in said pad trench.

IN THE ABSTRACT:

At page 13, replace the abstract beginning at line 2 with the following:

A semiconductor device includes an insulating film. On this insulating film, are formed [are] an interconnection trench communicating with a semiconductor element and a pad trench communicating with the interconnection trench. In the pad trench, a protrusion is formed by leaving one part of the insulating film. A conductive film is formed over the insulating film including the interconnection and pad trenches. Thereafter, the conductive film is removed by a CMP process. At this time, the protrusion serves to prevent the conductive film in the pad trench from being over-polished.

REMARKS

The Office Action mailed April 9, 2001 and the references cited therein have been carefully considered. Figures 1-5, the specification, Claims 1, 8, and 9, and the abstract have been amended in a sincere effort to further clarify the subject matter Applicants regard as the invention. In addition, Claims 7 and 14 have been cancelled without prejudice.

No new matter has been added to the drawings, specification, claims, or abstract, as amended. Support for this Amendment is found generally within the specification, claims, and drawings, as filed. As a result of this Amendment taken together with the remarks set

forth below, it is respectfully submitted that pending Claims 1-6 and 8-13 are now before the Examiner in condition for favorable consideration and allowance.

The Examiner has objected to Figures 1-4 as requiring a legend, such as "Prior Art", contending that only that which is known in the art is illustrated. In addition, the Examiner has objected to the drawings as failing to show a damascene interconnection 11, as referred to on page 4, line 19 of the specification.

In accordance with the Examiner's suggestion, provided herewith is a marked-up copy of Figures 1-5 with the proposed changes added to the figures. It is respectfully requested that the Examiner approve the changes to Figures 1-5, and upon such approval, such changes will be incorporated in the formal drawings. A Request for Approval of Drawing Changes on a separate sheet, along with an additional copy of the drawings, marked in red showing the changes to Figures 1-5, are submitted herewith. Thus, it is respectfully requested that the objections to the drawings be reconsidered and withdrawn.

The specification has been objected to due to various informalities, such as typographical errors and grammatical errors, and Claim 9 has been objected to due to its dependency upon itself. Accordingly, the specification has been amended throughout to correct typographical and grammatical errors, and Claim 9 has been amended to depend from Claim 8. Therefore, it is respectfully requested that the objections to the specification and Claim 9 be reconsidered and withdrawn.

Claims 1-6 and 8-13 have been rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 5,602,423 to Jain (*Jain*). The Examiner contends that *Jain* discloses a damascene interconnection including a conductor-filled trench (interconnection trench) 64 and insulating pillars (protrusions) 50, and that Figure 10 shows a plan view of a pillared landing pad (pad trench) 55 through which multiple protrusions are dispersed. Regarding Claims 4 and 11, the Examiner contends that element 38 in Figure 3 shows and column 6, lines 45-53 states that many other insulating patterns may be construed that produce the same

effect, that is, the reduction of dishing by the narrowing of wide trenches in a damascene interconnection.

Claim 7 and 14 have been rejected under 35 U.S.C. §103(a) as being unpatentable over *Jain* in view of U.S. Patent No. 5,854,140 to Jaso, et al. (*Jaso*). Specifically, the Examiner contends that although *Jain* does not show a damascene interconnection including a contact hole formed in a pad trench electrically connecting a conductive film and another conductive film arranged in a level lower than an insulating film, *Jaso* shows (in Figure 8) a semiconductor device including interconnects formed by a damascene process wherein an aluminum layer 26 is connected to a lower conductive metal layer 14 by way of a filled metal via 18. The Examiner further contends that it would have been obvious to one of ordinary skill to include the metal via and conductive metal layer described in *Jain* to connect the conducting segments of the *Jain* invention to an underlying conductor within the substrate, as shown by *Jaso*.

Jain relates to a semiconductor device that uses an embedded pillar to prevent damage, such as dishing, smearing, and overetching, to damascene connectors during fabrication, particularly where such conductors are relatively large. The device includes an insulating layer formed on a substrate having a substantially planar upper surface with a plurality of channels formed therein. The channel includes contiguous narrow channel segments enclosing one or more pillars, which have a top surface substantially coplanar with the upper surface of the insulating layer. In one embodiment, the pillar is formed integrally as part of the insulating layer. In an alternative embodiment, the pillar may be formed from an additional insulating or conducting layer.

However, nothing in *Jain* would teach or suggest contact holes at the bottom of the conductive film to enable division of the conductive film into non-contiguous areas, as now defined by amended Claims 1 and 8; disclosed on page 8, line 23 through page 10, line 11 of the specification; and shown in Figures 10-13. In addition, *Jain* fails to recognize that the increase in electrical resistance due to a decrease in the volume of the electrically conductive

material in the pad trench creates a problem, and that in order to prevent or substantially suppress this resistance from increasing, a contact hole may be formed in the pad trench to connect the conductive film to a further conductive film below an insulating film, as now defined by amended Claims 1 and 8.

Jaso relates to a method of forming aluminum contacts with a metal stop layer deposited prior to or following deposition of the aluminum. The metal stop layer is sufficiently thick enough to effectively allow a chemical-mechanical process to remove and planarize excess aluminum without exposing an underlying silicon dioxide layer.

However, nothing in *Jaso* would teach or suggest the use of pillars to counteract dishing in a single channel caused by overpolishing the conductive film. Specifically, *Jaso* merely describes two separate channels without pillars, as shown by element 26 in Figure 7, and that the metal stop layer suffices to counteract dishing, as shown in Figure 8. Thus, not only does *Jaso* not teach the use of pillars to avoid dishing, but teaches an entirely different and alternative approach to avoiding dishing, that is, the use of an additional step in applying a supplemental metal stop layer.

Further, nothing in either of the cited references would teach or suggest dividing the conductive film into non-contiguous areas and using contact holes to overcome the resulting conductivity problem between the non-contiguous areas and compensate for the increase in resistivity caused by dividing these areas, as now defined by amended Claims 1 and 8. In addition, although *Jaso* discloses the trench in which the contact hole is formed, Jaso does not teach or suggest a pillar provided within the trench nor that it is possible to prevent an increase in resistance due to the pillar by forming a contact hole, as now defined by amended Claims 1 and 8.

Applicants respectfully note that in order to support a claim of *prima facie* anticipation, a single reference must teach or enable each of the claimed elements as arranged in the claim interpreted by one of ordinary skill in the art. Further, in order to support a claim

of prima facie obviousness, the cited references must teach or suggest each and every element of the invention, and there must be a motivation in the references or the prior art to combine the references as suggested. However, none of the art of record teaches or suggests, either alone or in combination, a damascene interconnection including a contact hole formed within a pad trench to electrically connect a conductive film to a further conductive film formed below an insulating film, thereby substantially suppressing an increase in electrical resistance of the pad trench due to the formation of one or more protrusions, as now defined by amended Claims 1 and 8.

Applicants respectfully submit that Claims 2-6, which depend from Claim 1, and Claims 9-13, which depend from Claim 8, are patentable over the art of record by virtue of their dependency from Claims 1 and 8, respectively, which are believed patentable for the reasons set forth above. Further, Applicants submit that Claims 2-6 and Claims 9-13 define additional patentable subject matter in their own right. Therefore, it is respectfully requested that the rejection of Claims 1-6 and 8-13 under 35 U.S.C. §102(e) and the rejection of Claims 7 and 14 under 35 U.S.C. §103(a) be reconsidered and withdrawn.

In view of the foregoing Amendment and remarks, entry of the amendments to Figures 1-5, the specification, Claims 1, 8, and 9, and the abstract; favorable consideration of Claims 1, 8, and 9, as amended; favorable reconsideration of Claims 2-6 and 9-13; and allowance of pending Claims 1-6 and 8-13 are respectfully and earnestly solicited.

Respectfully submitted,

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VERSION OF AMENDMENT WITH MARKINGS TO SHOW CHANGES MADE

IN THE DRAWINGS:

Please approve the corrections to Figures 1-5, as shown in the marked-up copy of the same submitted herewith. A Request for Approval of Drawing Changes, on a separate sheet, and an additional copy of Figures 1-5, marked in red showing the changes to Figures 1-5 are submitted herewith.

IN THE SPECIFICATION:

At page 1, replace the paragraph beginning at line 11 with the following:

Recently, a so-called [the] damascene process has [being] been adopted [in providing] to provide multilevel interconnections for a semiconductor device having a metal or conductive film buried in the insulating film.

At page 1, replace the paragraph beginning at line 22 with the following:

It is known that, where [removing] the conductive film 5 is removed by the CMP process, [the greater is] as the opening area of the trench [the higher is] increases, the polish rate on the conductive film buried in the trench increases, as shown in Figure 2. [There encounters no especial problem in] In regions having a small trench opening area, such as is customary in [usual] interconnections, there are no particular problems. However, in regions having a large trench opening area, such as a bonding pad 6 shown in Figure 3, the conductive film 5 in the trench is polished into a dish-like form by an abrasive as shown in Figure 4, thus resulting in so-called dishing. Due to this, there are cases [that disconnection] a disconnect or an increase of resistance occurs in a central portion A where the wall thickness is reduced when providing connection between the bonding pad and the IC frame.

At page 2, replace the paragraph beginning at line 11 with the following:

Another object of the invention is to provide a damascene interconnection capable of preventing increases in resistance value [increase] or [disconnection] disconnects caused by dishing in a bonding pad, and a semiconductor device using the same.

At page 3, replace the paragraph beginning at line 2 with the following:

When removing the conductive film by a CMP process or the like, the protrusion dividing the pad trench serves as a stop [of] for polishing by an abrasive. Consequently, so-called dishing will not occur such that the conductive film in the pad trench is excessively removed. Thus, according to the invention, it is possible to prevent [a bonding pad from being increased of] increases in resistance or [causing disconnection] disconnects resulting from dishing on a bonding pad.

At page 3, replace the paragraph beginning at line 21 and ending at page 4, line 11 with the following:

Figure 1 is an illustrative view showing a process for a general damascene interconnection;

Figure 2 is a graph showing a usual polish characteristic in CMP;

Figure 3 is an illustrative view showing a prior art bonding pad;

Figure 4 is a sectional view [on] taken along line [IV-IV] X-X in Figure 3;

Figure 5 is an illustrative view showing one embodiment of the present invention;

Figure 6 is a sectional view [on] taken along line VI-VI in Figure 5;

Figure 7 is an illustrative view showing a method for forming the Figure 5 embodiment;

Figure 8 is an illustrative view showing another embodiment of the invention;

Figure 9 is an illustrative view showing another embodiment of the invention;

Figure 10 is an illustrative view showing another embodiment of the invention;

Figure 11 is a sectional view on line XI-XI in Figure 10;

Figure 12 is an illustrative view showing another embodiment of the invention; and

Figure 13 is an illustrative view showing another embodiment of the invention.

At page 4, replace the paragraph beginning at line 14 with the following:

A semiconductor device 10 of [this] the embodiment shown in Figure 5 and Figure 6 includes a semiconductor substrate 12 formed, for example, of silicon (Si) or the like. Note that the semiconductor substrate 12 may [use any of] be other materials. Semiconductor elements, including active and/or passive elements, are formed on the semiconductor substrate 12, although they are not shown in the figure.

At page 4, replace the paragraph beginning at line 19 with the following:

The semiconductor device 10 comprises a damascene interconnection 11 including, on the semiconductor substrate 12, an interconnection trench 16 extending from the semiconductor element (not shown) and a pad trench 18 connected to the interconnection trench 16. That is, an insulating film 14 is formed, for example, of silicon oxide (SiO_2) in a uniform film thickness on the semiconductor substrate. In the insulating film 14, the interconnection trench 16 and the pad trench 18 connected therewith are formed. The insulating film 14 may [use any of] be other materials.

At page 5, replace the paragraph beginning at line 1 with the following:

Note that Figure 5 and Figure 6 illustrate the insulating film 14 formed directly on the surface of the semiconductor substrate 12 in order [for simplifying] to simplify illustration and explanation. However, in the actual semiconductor device, one or a plurality of semiconductor element layers are formed on the semiconductor substrate 12, as is well known in the art, and an interconnection [layers] layer is formed as required on each of such

semiconductor element layers. The interconnection trench 16 provides electrical connection between the semiconductor element (not shown) and the pad trench 18. The pad trench 18 serves as a bonding pad on which wire-bonding is to be made to a not-shown IC leadframe. That is, the pad trench 18 is a connection terminal to provide electric conduction of the semiconductor element on each layer to and from the IC leadframe.

At page 5, replace the paragraph beginning on line 15 with the following:

In this embodiment, however, the following [devising] devise is implemented on the pad trench 18 with a comparatively large [in] opening area, in order to prevent [against] dishing as stated before. That is, the pad trench 18 has an insulating film 14 formed to be left as an island-spotted form. Consequently, the pad trench 18 is divided into unitary portions by island protrusions 20. However, the island protrusions 20 do not separate one portion from another portion of the pad trench 18, i.e. the pad trench 18 is continuous in areas except for the island protrusions 20. That is, the pad trench 18 in this embodiment has a large opening size but is reduced in its substantial opening area by the presence of the island protrusions 20. Specifically, in this embodiment the pad trench 18 has a side determined as approximately 50 - 200 μm and an interval of the protrusions 20 determined as approximately 5 - 20 μm.

At page 6, replace the paragraph beginning on line 9 with the following:

Hereunder, explanation is made on a method to concretely manufacture a semiconductor device 10 of the embodiment having a damascene interconnection 11 as described above, with reference to Figure 7. Incidentally, in Figure 7, an insulating film 14 is formed directly on a surface of a semiconductor substrate 12. It should however be noted that the semiconductor device 10, in [practical] practice, has a proper number of semiconductor element layers as stated before and Figure 7 depicts an interconnection structure having only one layer for the sake of convenience.

At page 6, replace the paragraph beginning on line 25 and ending at page 7, line 14 with the following:

In the CMP process, the semiconductor substrate 12 (including the insulating film 14 and the conductive film 22) is urged onto a polishing pad mounted on a polisher table. The table and the substrate holder are relatively rotated while supplying to the polishing pad a slurry containing abrasive particles. When the conductive film 22 on the insulating film 14 is removed, the polishing operation is finished. In this case, the abrasive particle for polishing is selected of a kind (material, particle size, etc.) such that in CMP a polish rate on the insulating film 14 is lower than a polish rate on the conductive film 22. According to an experiment conducted by the present inventors, the polish rate in concrete is desirably given as (polish rate on the conductive film 22) / (polish rate on the insulating film 14) $\geq$ 20 to 10. This is because in CMP the conductive film 22 on the insulating film 14 needs to be removed as [rapid] rapidly as possible. However, the insulating film 14 should be prevented from being damaged due to polishing, and the island projections 20 are to prevent [over-polish to] over-polishing the conductive film 22 of the pad trench 18. Consequently, there is a necessity of providing the insulating film 14 with greater polish resistance than that of the conductive film 22.

At page 7, replace the paragraph beginning on line 15 with the following:

According to this embodiment, in the process of removing the conductive film 22 (Figure 7(d)), the protrusions 20 (insulating film 14) having a low polish rate [acts] act such that the conductive film 22 is decelerated [in proceeding] during the process of polishing by the polish pad. Thus, the conductive film 22 in the pad trench 18 can be prevented from being removed to an excessive extent. This in turn makes it possible to prevent the pad trench 18 from increasing in resistance or the occurrence of [disconnection] disconnects due to dishing.

At page 7, replace the paragraph beginning on line 21 and ending at page 8, line 3 with the following:

That is, in the conventional art shown in Figure 3 and Figure 4, because the pad trench 6 is contacted in its entire opening by a polish pad (not shown), the pad trench 6 having a large opening area is partly over-polished [into a result of] resulting in dishing. On the contrary, in this embodiment, despite the pad trench [entirely] is large in an opening area, the opening is divided into unitary portions wherein the opening area is small if considered on a portion sandwiched between the island protrusions 20. Due to this, over-polish will not occur. As a result, a conductive film 22 in the pad trench 18 is given a planar surface as shown in Figure 6 and Figure 7(d).

At page 8, replace the paragraph beginning on line 4 with the following:

In this manner, in the present invention, where using a CMP method having a polish characteristic that the polish rate increases with an increase in the opening area, the forming of protrusions in the pad trench reduces the substantial opening area, thereby preventing dishing.

At page 8, replace the paragraph beginning on line 11 with the following:

That is, in the embodiment shown in Figure 8, a plurality of protrusions or ridges 20 are formed extending from respective outer edges of four sides of a rectangular pad trench 18. It should be noted that, in also this case, the other areas of the pad trench 18 are continuous with one another. In also this embodiment, the substantial opening area is reduced in the areas [of] between the protruding ridges 20, between protruding ridges extending from different sides, and between the protruding ridge 20 and the inner edge of the pad trench 18.

At page 8, replace the paragraph beginning on line 18 with the following:

In the embodiment of Figure 9, a pad trench 18 has one ridge 20 formed in a squared-spiral form. In the Figure 9 embodiment, because the ridge 20 is in the spiral form, the pad trench 18 is not divided into non-continuous areas. In this manner, by forming the ridge 20 in the spiral form, the opening area is substantially reduced in the areas [of] between portions of the ridge 20 and between the ridge 20 and the pad trench 18 inner edge.

At page 9, replace the paragraph beginning on line 2 with the following:

Explanation is made in detail on an embodiment having contact holes 26 formed through the insulating film 14, with reference to Figure 10 and Figure 11[,]. This embodiment is to be applied to a semiconductor device having another layer formed in a level lower than the insulating film 14, as shown in Fig. 11. That is, another insulating film 28 is formed on a semiconductor substrate 12, and further another conductive film 30 is formed on the insulating film 28. The insulating film 14 is formed on the conductive film 30. In a bottom of the pad trench 18, a plurality of contact holes 26 are formed penetrating through the insulating film 14. When forming a metal or conductive film 22 in the pad trench 18, a metal or conductive material thereof is also filled in the contact holes 26 to provide electrical connection between the upper-leveled conductive film 22 and lower-leveled conductive film 30. By thus forming the contact holes 26 in the pad trench 18 and connecting [between] the conductive films 22 and 30, it is possible to eliminate the disadvantage as feared upon forming protrusions 20 in the pad trench 18.

At page 9, replace the paragraph beginning on line 15 with the following:

That is, the protrusions or ridges, if formed in the pad trench 18 [results] , result in a volume decrease of the pad trench 18, i.e. volume reduction of the conductive film 22 of the pad trench 18. It is to be feared that the bonding pad may be increased in electric resistance by the volume reduction in the conductive film 22 of the pad trench 18. However, the conductive film 22, if coupled to the conductive film 30 as in the Figure 10 and Figure 11

embodiments, increases the effective volume of the conductive film 22, thus properly suppressing the electric resistance from increasing.

At page 9, replace the paragraph beginning on line 25 and ending at page 10, line 11 with the following:

In an embodiment of Figure 13, a ridge 20 is formed in a closed-loop form in a manner different from the Figure 9 embodiment. Accordingly, in this embodiment, the conductive film 22 of the pad trench 18 is divided into portions, in a manner different from the above embodiment. In this case, the contact holes 26 are especially effective. That is, the formation of contact holes 26 connects the conductive film 22 of the pad trench 18 to a lower-leveled conductive film 30 (Figure 11). Consequently, the divided portions of the conductive film 22 of the pad trench 18 are electrically coupled together through the conductive film 30. That is, in the Figure 13 embodiment, the ridge or protrusion 20 is formed in a closed-loop form. However, [there encounters] no problem is encountered with [disconnection] disconnects in the pad trench 18 due to the protrusion or ridge 20 because the conductive film 22 is coupled to the lower-leveled conductive film through the via holes 26.

IN THE CLAIMS:

Please cancel Claims 7 and 14 without prejudice.

Please amend Claims 1, 8, and 9 by rewriting the same as follows:

1. (Amended) A damascene interconnection comprising:

an interconnection trench formed in an insulating film and a pad trench communicating therewith;

a protrusion formed by a portion not removed of said insulating film in said pad trench to decrease a substantial opening area of said pad trench; [and]

a conductive film buried in said interconnection trench and said pad trench; and

a contact hole formed within said pad trench to electrically connect said conductive film to a further conductive film formed below said insulating film, wherein said contact hole and said further conductive film substantially suppress an increase in electrical resistance in said pad trench due to formation of said protrusion.

8. (Amended) A semiconductor device, comprising:

a semiconductor substrate;

an insulating film formed on said semiconductor substrate;

an interconnection trench formed on said insulating film and communicating with a semiconductor element;

a pad trench formed on said insulating film and communicating with said interconnection trench;

a protrusion formed by a portion of not removed of said insulating film in said pad trench and reducing a substantial opening area of said pad trench; [and]

a conductive film buried in said interconnection trench and said pad trench;

a further conductive film formed below said insulating film; and

a contact hole formed within said pad trench to electrically connect said conductive film to said further conductive film, wherein said contact hole and said further conductive film substantially suppress an increase in electrical resistance in said pad trench due to formation of said protrusion.

9. (Amended) A semiconductor device according to claim [9] 8, wherein said protrusion is formed not to divide said conductive film buried in said pad trench.

IN THE ABSTRACT:

At page 13, replace the abstract beginning at line 2 with the following:

A semiconductor device includes an insulating film. On this insulating film, are formed [are] an interconnection trench communicating with a semiconductor element and a pad trench communicating with the interconnection trench. In the pad trench, a protrusion is formed by leaving one part of the insulating film. A conductive film is formed over the insulating film including the interconnection and pad trenches. Thereafter, the conductive film is removed by a CMP process. At this time, the protrusion serves to prevent the conductive film in the pad trench from being over-polished.